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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Christoph Wasshuber, et al.	Docket No:	TI-31016
Serial No:	10/020,111	Conf. No:	5837
Examiner:	Richard A. Booth	Art Unit:	2812
Filed:	12/14/2001		
For:	METHODS AND APPARATUS FOR INDUCING STRESS IN A SEMICONDUCTOR DEVICE		

#11 Appeal Brief 8/8/03

APPEAL BRIEF UNDER 37 C.F.R. 1.192

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that this Appeal Brief filed, in triplicate, under 37 CFR 1.192 is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 8-4-03.

Ann Trent
Ann Trent

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Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the final rejection mailed March 6, 2003, and the Advisory Action mailed May 21, 2003.

Real Party in Interest under 37 C.F.R. 1.192(c)(1)

Texas Instruments Incorporated is the real party in interest.

Related Appeals and Interferences under 37 C.F.R. 1.192 (c)(2)

There are no related appeals or interferences known to appellant, the appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the board's decision in the pending appeal.

Status of Claims on Appeal under 37 C.F.R. 1.192 (c)(3)

The application was originally filed with claims 1-13. Claims 15-22 were withdrawn from consideration pursuant to a restriction requirement, claims 1-12 and 23-28 were cancelled and claims 29-38 were added. On June 6, 2003 the appellant appealed from the final rejection of claims 29-38.

Status of Amendments Filed After Final rejection under 37 C.F.R. 1.192 (c)(4)

No amendments were filed after the final rejection.

Summary of the Invention under 37 C.F.R. 1.192(c)(5)

Appellant's invention comprises a method of forming a MOS transistor by implanting a species beneath the channel region of the MOS transistor so as to induce stress in the MOS transistor region. With reference to Figure 1 in appellants disclosure, a gate oxide structure 30, a poly gate structure 31, and a conductive gate contact structure 32 are formed over a semiconductor substrate 14 (page 6, lines 29-31). Source and drain regions 22a and 22b are formed in the substrate leading to the formation of a channel region 24 beneath the conductive gate contact. (page 6, lines 22-28). Stress is induced in the MOS transistor by forming regions 12a and 12c beneath the source and drain regions 22a and 22b by implanting species comprising carbon, germanium, and/or oxygen. (page 7, lines 16-24). Furthermore a third implanted region 12b is formed by implanting the above described species of germanium, carbon, and/or oxygen beneath the channel region 24 to induce stress in the channel region (page 7, lines 17-19). Figure 1 and the accompanying text clearly differentiate the drain and source regions from the channel region and define three implanted regions 12a, 12b, and 12c beneath these regions.

Statement of Issues Presented for Review under 37 C.F.R. 1.192 (C)(6)

Are claims 29-38 properly rejected under 35 U.S.C. 102(b) as being anticipated by Kawasaki et al., U.S. Patent 5,514,902?

Statement of the Grouping of Claims under 37 C.F.R. 1.192(C)(7)

(a) Claims 29 to 31 and 35 to 38 stand or fall together.

(b) Claims 32 to 34 stand or fall together.

The Examiner's Rationale

The examiners rationale for rejecting claims 29-38 under 35 U.S.C. 102(b) as being anticipated by Kawasaki et al., U.S. Patent 5,514,902 was stated as follows in his final rejection dated March 2, 2003:

Kawaski et al. shows the invention as claimed including providing a semiconductor 1; forming a MOS transistor source region 8a in said semiconductor; forming a MOS transistor drain region 8b is said semiconductor; and implanting a species 7a, 7b containing carbon (see col. 2-line 61 to col. 3-line 10) beneath the channel region to induce a compressive stress into the channel region (see Figs. 1-9 and their description).

Arguments

I. Are claims 29-38 properly rejected under 35 U.S.C. 102(b) as being anticipated by Kawasaki et al., U.S. Patent 5,514,902?

Appellants contend that claims 29-38 are not properly rejected under 35 U.S.C. 102(b) as being anticipated by Kawasaki et al., U.S. Patent 5,514,902.

Claim 29 comprises the limitation of implanting a species in said semiconductor beneath said MOS transistor channel region so as to induce stress in said MOS transistor channel region. The examiner in forming the rejection contends that the Kawasaki et al. patent (herein after Kawasaki) describes implanting a species 7a, 7b containing carbon beneath the channel region to induce a compressive stress into the channel region. The examiners interpretation of the Kawasaki patent is incorrect as will be explained below.

Figures 1-9 of Kawasaki describe a process for implanting nitrogen into regions adjacent to the gate structure and not in the channel region as stated by the examiner.

With reference to Figure 6 in Kawasaki, a resist structure 12 is formed on the gate electrode 4 and nitrogen is ion-implanted into silicon substrate 1 using resist 12, sidewall oxide film 5 and isolation oxide film 2 as a mask. The implanted regions are shown as 7a and 7b in Figure 7 of Kawasaki. A cursory examination of Figure 7 might suggest that the implanted species extend under the gate and into the channel region but this is not the case. Following the implantation of the nitrogen species, the dopant used to form the source and drain regions is implanted. This is shown in Figure 8 of Kawasaki by the implantation of boron to form regions 8a and 8b. Following the implantation of boron, a thermal anneal is performed which causes the boron to diffuse outwards and the implanted nitrogen to diffuse towards the surface of the semiconductor. This is described in column 7, lines 13 to 29. It is well defined in the semiconductor arts that the metallurgical junction between the source and drain regions and the channel region is the point where the doping in the channel region is equal to the doping in the source and drain regions. This point will be determined by: (a) how far the boron (or other doping species) diffuses into the region under the gate, and by (b) the doping of the region under the gate electrode 4. There is no information regarding the doping of the region under the gate electrode in Kawasaki and so it is not possible to determine precisely the position of the metallurigal junction. However an examination of Figure 11 shows a depth of approximately 2.5 to 3um for the measurable implanted nitrogen following an annealing process. The depth of the implanted boron following the anneal is shown in Figure 13 to be on the order of 3um at a concentration of 10^{16} cm^{-3}. Figures 11 and 13 imply that the nitrogen and boron in the source and drain region overlap after the annealing process. Therefore given that the channel region starts when the boron concentration falls below that of the doping concentration in the channel region, it is clear from Figures 11 and 13 that the nitrogen is not implanted in the channel region. The nitrogen is implanted in the source and drain region which is fully defined after the outward diffusion of boron and the inward diffusion of nitrogen.

Furthermore claim 29 comprises the limitation that the implanted species induce stress in said MOS transistor channel region. It is well established that the implantation conditions will determine whether stress is induced in the adjacent regions. The intent of

the implantation in Kawaski is to reduce the boron diffusion during thermal annealing. As such the position of the nitrogen implant and the conditions under which the implant is performed (i.e. energy and dose) are designed to reduce the diffusion. The amount of nitrogen (or carbon) implanted in the source and drain regions adjacent to the gate electrode will not induce stress in the adjacent channel region.

Claim 29 is allowable over Kawaski for the reasons stated above. In addition dependent claims 30 and 31 depend from claim 29 and are also allowable over the Kawaski et al. patent.

Claim 35 comprises the limitation of implanting a species in said semiconductor beneath said MOS gate structure so as to induce stress in said first region and is therefore also allowable over Kawaski for the reasons stated above. In addition claims 36, 37, and 38 depend from claim 35 and are also allowable over the Kawaski et al. patent.

Claims 32 comprises the limitation of implanting a species in said semiconductor confined to a region substantially beneath said MOS transistor channel region so as to induce stress in said MOS transistor channel region. This is illustrated in Figure 1 of the disclosure on appeal where the implanted region 12b is shown substantially beneath the channel region 24. Kawaski discloses implanting species into the source and drain region. Species implanted into the source and drain region cannot exist substantially beneath the MOS channel region and so claim 32 is allowable over Kawaski. In addition claims 33 and 34 depend on claim 32 and are also allowable over the cited art.

II. Why Appellant believes the claims of two groups to be separately patentable

Claim 32 limits the implanting a species in said semiconductor confined to a region substantially beneath said MOS transistor channel region so as to induce stress in said MOS transistor channel region. Claims 29 and 35 limit the implanting a species in said semiconductor beneath said MOS transistor channel region so as to induce stress in said MOS transistor channel region. "Substantially beneath the channel" is more limiting than

"beneath the channel" which includes any region of the channel. Claim 32 and its dependent claims 33 and 34 are therefore separately patentable.

Conclusion

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 29-38 under 35 U.S.C. § 102 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,

Peter McLarty
Reg. No. 44,923
Attorney for Appellants

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APPENDIX

Claims on Appeal

29. A method for forming a MOS transistor, comprising:

providing a semiconductor;

forming a MOS transistor source region in said semiconductor;

forming a MOS transistor drain region in said semiconductor;

forming a MOS channel region in said semiconductor between said source region and said drain region; and

implanting a species in said semiconductor beneath said MOS transistor channel region so as to induce stress in said MOS transistor channel region.

30. The method of claim 29 wherein said species is selected from a group consisting of oxygen, germanium, and carbon.

31. The method of claim 29 wherein carbon is implanted beneath said MOS transistor channel region to induce a compressive stress in said MOS transistor channel region.

32. A method for forming a MOS transistor, comprising:

providing a semiconductor;

forming a MOS transistor source region in said semiconductor;

forming a MOS transistor drain region in said semiconductor;

forming a MOS channel region in said semiconductor between said source region and said drain region; and

implanting a species in said semiconductor confined to a region substantially beneath said MOS transistor channel region so as to induce stress in said MOS transistor channel region.

33. The method of claim 32 wherein said species is selected from a group consisting of oxygen, germanium, and carbon.

34. The method of claim 32 wherein carbon is implanted beneath said MOS transistor channel region to induce a compressive stress in said MOS transistor channel region.

35. A method for forming a MOS transistor, comprising:

providing a semiconductor;

forming a gate oxide layer on said semiconductor;

forming a MOS transistor gate structure on said gate oxide layer above a first region in said substrate; and

implanting a species in said semiconductor beneath said MOS gate structure so as to induce stress in said first region.

36. The method of claim 35 wherein said MOS transistor gate structure comprises polysilicon.

37. The method of claim 36 wherein said species is selected from a group consisting of oxygen, germanium, and carbon.

38. The method of claim 36 wherein carbon is implanted beneath said MOS transistor gate structure to induce a compressive stress in said MOS transistor channel region.